Junction Development for HTS Waveform Generator Circuits

J. M. Murduck, J. Talvacchio, D. A. Kahler, A. Kirschenbaum, and D. L. Miller

Abstract—**HTS digital-to-analog converter circuits designed to generate complex, low-noise waveforms at GHz frequencies have special requirements for Josephson junction parameters and integration of junctions in a microwave circuit. We developed an eight-mask process integrating two HTS layers forming our edge SNS junctions with YBCO electrodes and cobalt-doped YBCO N-layers and parts of the circuit that were laid out in coplanar waveguides. Other layers use silver films and low-loss silicon dioxide depositions to form coaxial and stripline transmission lines and RF filters. A molybdenum resistor layer is also included for 50-ohm terminations. Innovative process steps allowed us to obtain low I_cR_n products of 24 mV at 60-65K with critical currents of 1-2 mA to match the Josephson frequency to input signals at 12 GHz. A desire to integrate more than 200 junctions in a one-dimensional array that behaves as a lumped circuit element led to new masking techniques to reduce the spacing between edge junctions to 3 microns.**

Index Terms—**superconducting devices, high-temperature superconductors, signal generators**

I. Introduction

A Josephson junction array, based on the Josephson voltage standard can provide a low-noise digital-to-analog converter for radar applications. It is proposed that as few as 100 junctions in a series-array are needed to derive a digital waveform that has -150 dBc/Hz performance [1]. This waveform generator circuit puts particular constraints on junction fabrication and performance. Variation in junction critical current will degrade the circuit's signal-to-noise ratio. In addition, the junctions must be physically contained in much less than a quarter-wavelength of the rf signal in order not to destructively interfere with one another. Also, the I_cR_n product of these junctions must be targeted to match their Josephson frequency with the rf frequency of the input signal.

These requirements constrain our HTS integrated circuit process and we will show how these are addressed in our junction fabrication development.

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II. Process Flow

A custom process flow was designed in order to balance circuit requirements with process yield. This application requires a variety of circuit functions including a series array of Josephson junctions, microstrip line, coplanar waveguide and resistor elements (Fig. 1). Although some advantage is gained by increasing the number of epitaxial superconducting layers, it correspondingly reduces the circuit yield in order to achieve sufficient critical current of crossovers, dielectric integrity and oxygenation of underlying layers of YBCO.

The strategy employed for this application was to use the YBCO depositions primarily for junction fabrication. Other circuit elements were achieved by use of non-epitaxial dielectric and normal metal depositions. The dielectric material that was chosen was bias-sputtered SiO_2 both due to its low-loss and that its deposition on our Josephson junctions could be done without deleterious effect to the resulting

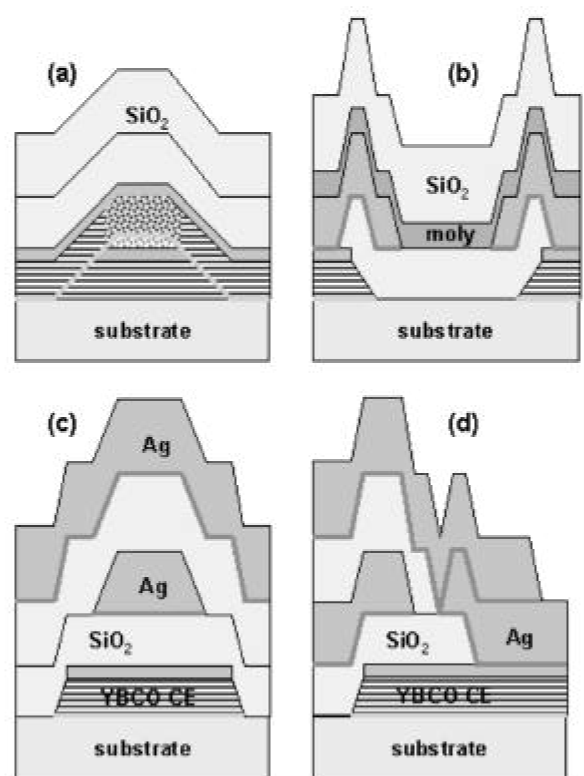

Fig. 1. Process cross-section for critical circuit elements: a) Josephson junctions embedded in a coplanar waveguide, b) 50 Ω resistor, c) impedance-matching circuit element, and d) a 2 GHz filter.

junction properties. The normal metal was chosen to be silver due to its lower resistivity than gold and ease of deposition. The resistor material for this circuit was molybdenum with a titanium overlayer.

The initial choice of junction was the YBCO/Co-doped YBCO/YBCO edge junctions due to their reproducibility and within-wafer uniformity [2]. This junction consists of etching a YBCO film with a dielectric overlayer to form an edge with an angle of typically 15° to 35°. A barrier material is epitaxially deposited on the formed ramp-edge and followed by an in-situ YBCO counterelectrode. In addition, by choice of electrode and barrier material, the I_cR_n product of the resulting junction can be targeted to match the input signal frequency.

III. Junction Geometry

It is desirable to integrate as many junctions as possible within a series array that will electrically appear as a lumped-circuit element. For planar edge-junctions, there are practical limitations due to feature resolution in both photolithography and resulting etched structure. In addition, layer-to-layer alignment requires additional and unavoidable spacing to be included.

Similar circuits fabricated using Nb-based vertical junctions have similar requirements [1]. Linear junction density in that circuit is 0.11 jj/mm.

The edge junction geometry (Fig. 2) has necessary constraints in practical fabrication. Base electrodes feature-to-feature spacing must be a sufficient distance (d_1) to allow material to be entirely cleared during ion mill etching. The feature size of the base electrode in the direction of the linear array of junctions (d_2) must also be minimized in this process. Finally, the need for feature-to-feature isolation of the counter electrode (d_3) also contributes to the number of junctions that can be fabricated in a given length. Efforts to minimize these distances will be considered below.

IV. Base Electrode Spacing

The feature-to-feature spacing of the base electrode layer must take into account the angle of ion milling, mask height, and sufficient distance to ensure complete base electrode removal. The length of the ramp-edge contributes to the overall length and is a function of the angle of the ramp-edge. However, the ramp-edge angle is constrained to be less than 45 degrees to avoid grain boundary formation within the YBCO film.[3] In practice, edge angles of 35 degrees and less provide needed margin to ensure local structure along the ramp-edge doesn't exceed 45 degrees.

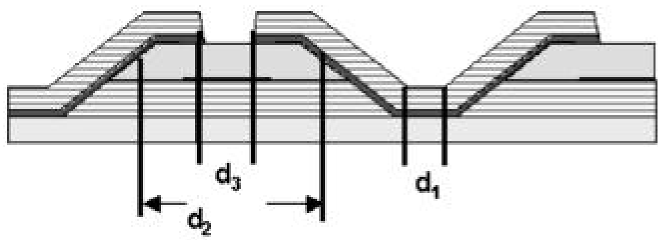

Fig. 2. Junction geometry with critical spacing: d_1 = spacing between base electrodes, d_2 = width of base-electrode mask, d_3 = spacing between counterelectrodes. The horizontally striped fill pattern indicates the cross section of c-axis-oriented YBCO films. The black film indicates Co-doped YBCO and the gray film shows the location of the base electrode insulator, typically $SrTiO_3$.

V. Base Electrode Length

Standard fabrication of base electrode features consist of masking using 1518 photoresist on the YBCO/$SrTiO_3$ bilayer. The photoresist edge profile is initially near vertical until it is postbaked at 130°C for 1 minute. As feature size decreases below 25 µm, the reflowed photoresist profile becomes a function of the base electrode feature size due to surface tension effects (Fig. 3). Reducing the mask height will reduce the effect of surface tension and can be readily accomplished by increasing the speed the photoresist is spun onto the wafer. However, this approach is limited by the thickness of the photoresist needed to withstand the length of the ion mill etch necessary to etch the YBCO/$SrTiO_3$ bilayer. The variation in photoresist edge angle results in a corresponding variation of the YBCO/$SrTiO_3$ bilayer using a simple isotropic etch model [4].

As feature sizes approach 4 to 8 µm, the length-scale desired for this application, the photoresist edge angle increases along with the resulting etched base electrode.

The edge angle is also highly dependent on the relative etch rate of the masking material and the film to be etched (Fig. 4).

An alternate approach to reduce the edge angle is to increase the mask-to-film Etch Rate Ratio (ERR). This can be

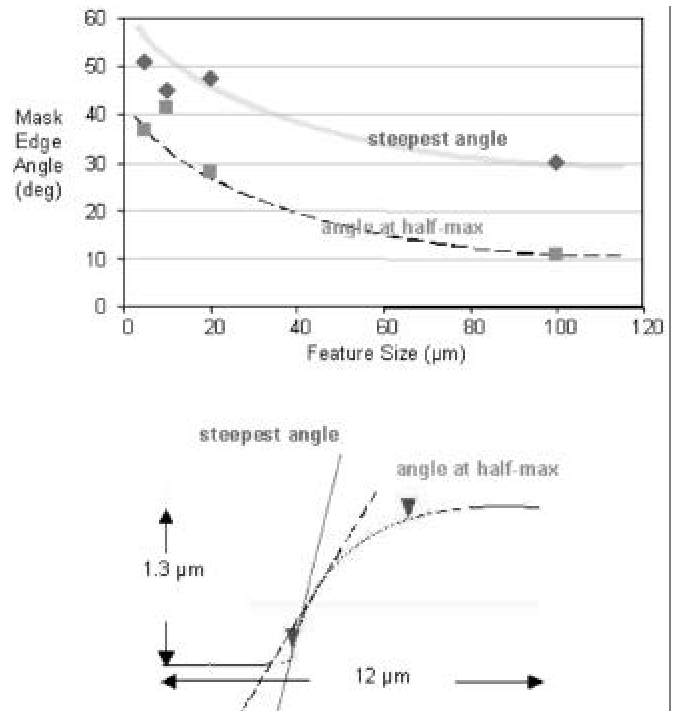

Fig 3. For reflowed photoresist, mask edge angle is a function of feature size. Edge angle were taken by Atomic Force Microscopy (AFM).

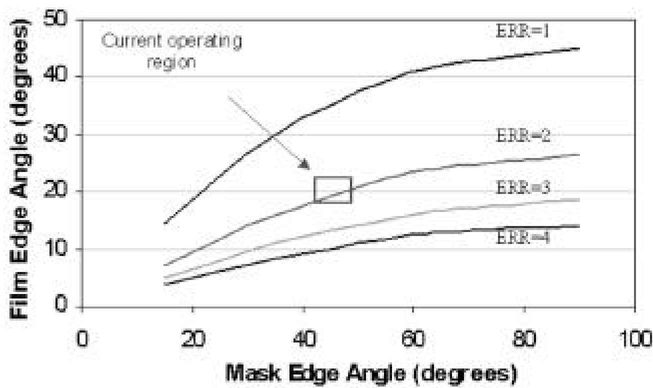

Fig 4. Using a simple isotropic model the mask edge angle is related to the resulting film edge angle for various values of mask-to-film Etch Rate Ratio (ERR).

done by including a partial pressure of oxygen along with argon during the ion milling process. This preferentially etches the photoresist as compared to the $YBCO/SrTiO_3$ bilayer. This technique was successfully used to obtain lower base electrode edge angles. However, the resulting YBCO edge was considerably roughened during this etch process. The edge smoothness is thought to be critical to junction performance [5] and as such these base electrodes were no longer optimal for subsequent junction fabrication.

A variety of approaches were compared in order to find the optimal method of reducing the base electrode feature size (Table I). A number of these methods were successful in producing the targeted edge angle of the $YBCO/SrTiO_3$ base electrode. For example, Reactive Ion Beam Etch (RIBE) using a photoresist mask and ion milling in an argon/oxygen gas mixture produced the desired geometry. However it consistently had artifacts along the edge including re-deposited "shards" and increased roughness along the edge. Modifying the photoresist profile in oxygen plasma again incurred increased roughness along the edge.

Another approach that demonstrated the capability of modifying the photoresist profile of small features was by varying the photoresist exposure at the edge of the base electrode feature. This was done with different two approaches: purposely defocusing the masking of the base electrode and by use of grayscale photolithography where the mask pattern consists of a half-tone gradient at the edges of the feature. Both these approaches demonstrated that the photoresist edge angle could be varied but in practice were difficult to control and reproduce.

Masking with photoresist and using a single-direction of ion milling was also considered. This approach would not be satisfactory for digital circuit fabrication due to parasitic inductance that would be incurred by interconnecting these junctions but could reasonably be implemented for this application. However, ion milling using this technique produced structure in the base electrode edge that was due to shadowing from "boulders" and other such defects along the top of the base electrode edge.

TABLE I
EDGE-ANGLE FORMATION PROCESSES COMPARISON

Approach	Pro	Con
Standard 130°C post-bake slumping	Good at large area base electrodes	Increasingly sharp edges for reduced base electrode size < 30 μm
Multilayer masking with thin Nb	Uniform edge angles as function of base electrode size	Resulting edges of both Nb and YBCO too steep; Nb only 2x thinner than PR
Sculpting Nb edge of multilayer mask	Adding O_2 to RIE recipe gave Nb edge angles under 30 degrees	YBCO edge angles too sharp due to reduced Nb mill rate relative to PR
RIBE with oxygen	Ion beam etching in O_2/Ar mixture controls PR etch rate	Resulting edges had shards, roughness
Pre-exposing PR to reduce PR	Can reduce PR edge angle down to 35°	Reduces PR thickness and hardens PR
Plasma etching of PR	Readily implemented	Creates greatly roughened PR edge
Out-of-focus masking	Readily implemented	Resolution quickly degraded past utility. Too demanding on litho tool
Grayscale photolithography	Reduce complexity; number of variables	Demanding mask-making
Single-direction ion milling	Reduce complexity; number of variables	Requires very shallow milling angles and precise alignment in ion mill
Multiple exposures of standard post-bake	Multiple exposures of standard post-bake process	Exposes patterned edges to PR so taxes edge cleaning process

The process approach that proved most successful and extendable to other circuit applications was utilizing our standard process of defining base electrode edges and iterating that process until the required junction density is achieved. As long as the photoresist mask is greater than 30 μm in length then the desired photoresist edge angle can be achieved. After ion milling, a second masking is then done to define further base electrode edges between the first set of etched edges. This method has the advantage of being able to increase the junction density that is limited primarily by the base electrode feature-to-feature spacing (d_1) and the length of the ramp edge of the base electrodes. The disadvantage of this approach is that the base electrode edges are exposed to different amounts of processing that can affect junction performance. Considerable study has been made to clean these edges via wet etching and ex-situ and in-situ ion milling once they are all fabricated in order that here would be no systematic variation in the junctions. The reproducibility of the edge geometry has been demonstrated on a single wafer with two different maskings of the base electrode.

VI. COUNTER-ELECTRODE SPACING

The counter-electrode must be aligned so as to entirely cover the base electrode and in addition be isolated from other counter-electrode features (d_3 in Fig. 2). This can be minimized by the addition of a "poison" layer deposited on the base electrode as shown in Fig. 5. A thin layer (30 nm) of

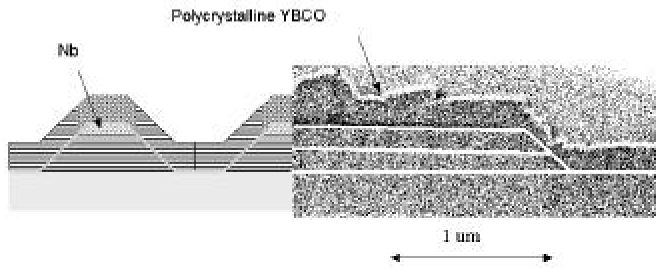

Fig 5. FIB cross-section and micrograph of polycrystalline YBCO growth on base-electrode structure with Nb overlayer. The white lines have been added to aid the eye. Note the increased roughness above the structure as compared to the YBCO film growth on the etched substrate to the right.

Nb was deposited ex-situ on the YBCO/$SrTiO_3$ bilayer. After base electrode definition, the subsequent YBCO counter-electrode epitaxy is destroyed and serves to isolate the counter-electrode features without need of precise alignment. The high-melting point Nb overlayer was observed to not diffuse through the $SrTiO_3$ into the YBCO. This self-aligned technique reduces the junction length by 3 µm per junction.

VII. Targeting Junction Parameters

Junctions have been targeted with relatively low I_cR_n products to match the input rf frequency. Since critical currents of 1-2 mA are needed to supply output power from the circuit, junction resistances need to be on the order of 0.012–0.024 O. Since a 10-nm thick normal-conducting layer of Co-doped YBCO has a resistance of about 0.01 O, any interface resistance or lack of interface transparency could cause us to exceed the targeted junction resistance. Fig. 6 shows how we use a Ag layer as a shunting conductor to make the targeting of junction resistance more robust. This Ag film thickness is set to provide optimal shunted-junction resistance and can be trimmed if needed after the fabrication has been completed.

The polycrystalline YBCO that is grown on the Nb layer creates considerable film roughness that could affect subsequent normal metal film growth (Fig. 5). Empirically, deposition of continuous normal metal over the counter-electrode has been achieved.

VIII. Conclusion

The operating frequency of our digital-analog converter circuit design sets constraining requirements on our HTS junction fabrication process. These include low-I_cR_n products, uniform critical current densities, reproducibility, and a high packing density of these junctions in a linear array. We applied a modification of our YBCO/Co-doped YBCO/YBCO edge junctions to meet these disparate requirements. Junction density was increased by use of a novel 'poison' layer that allows self-aligned deposition of the counter-electrode. Noble metal shunting of the counter-electrode is used to optimally impedance match and is a post-fabrication 'trimmable' process. Finally, ten methods were evaluated to best reduce the base-electrode feature size. An iterative strategy of

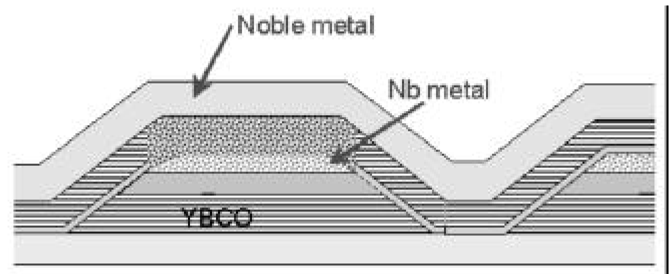

Fig 6. Noble metal (Ag) overlayer to the counter-electrode resistively shunts the junctions and allows some tuning of the low junction resistances needed for I_cR_n targets of 24 µV.

defining the base-electrode into increasingly small features was chosen. This approach accentuates the role of the cleaning of the base-electrode edge in order to maintain junction uniformity. By using these techniques, junction linear density can be increased from 0.03 to junctions/um to 0.2 junctions/µm, comparing favorably with the 0.11 junctions/um being used in comparable Nb-based circuits.

Acknowledgment

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